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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/802,857
Filing Date: March 12, 2001
Appellant(s): KOH ET AL.

Ronald P. Kananen
Brian K. Dutton
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on April 22, 2005.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of invention contained in the brief is correct.

(6) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(7) Prior Art of Record

5,454,100	SAGANE	9-1995
5,701,506	HOSOTANI	12-1997

(8) Grounds of Rejection to Be Reviewed on Appeal

The following ground(s) of rejection are applicable to the appealed claims:

Claims 13-25 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,454,100 to Sagane ("Sagane") in view of U.S. Pat. No. 5,701,506 to Hosotani ("Hosotani").

This rejection is set forth in a prior Office Action, mailed on November 19, 2004.

(9) Response to Arguments

At the outset, Appellant's arguments (Brief, pages 7-12), which are based on and shift back and forth between Sagane's first (FIG. 1) and second (FIG. 3) embodiments, seem to obfuscate the grounds of rejection actually set forth in the final Office Action. Rather, the rejections are based on the teachings of Sagane and Hosotani, in combination. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981) and *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The examiner has nonetheless attempted to address Appellant's arguments below.

Moreover, it is noted that claim 13 merely recites "a central processing unit receiving said plurality of coincidence signals." Appellant's arguments seem to imply that "receiving" should necessarily mean that the plurality of coincidence signals is directly connected or directly coupled to the central processing unit. This limitation is not recited in the claim. For example, Appellant states that "the Office Action fails to clearly identify within the second embodiment of

Sagane where and how the CPU 2 is to receive a plurality of coincidence signals, since signal A of comparator 8 found within figure 3 is applied to switch 23 and not to the CPU 2" (Brief, page 8, fifth paragraph). Appellant further states that "figure 1 of Sagane fails to disclose, teach or suggest the coincidence signal E being connected to the CPU 2" and states, "Instead, the comparator 8 for the first embodiment of Sagane supplies the interrupt control circuit 7d with a coincidence signal E via the switch 7c" (Brief, page 9, third paragraph). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

"Claims 13-18 and 21-25" (Brief, page 6).

Appellant acknowledges that the second embodiment of Sagane teaches that pluralities of comparators 8, correction address registers 21 and correction data registers 22 may be provided to address multiple bugs (Brief, page 8, second paragraph), but contends that "the second embodiment of Sagane fails to expressly state that each of the pluralities of comparators 8 described at column 7, line 1 of Sagane would necessarily output a coincidence signal" (Brief, page 8, fifth paragraph).

However, referring to the first embodiment illustrated in FIG. 1, Sagane expressly discloses that a comparator 8 outputs a coincidence signal E (see, for example, column 3, lines 48-52). In the second embodiment, a comparator 8 outputs a coincidence signal A (see, for example, FIG. 3). Both comparators 8 output a coincidence signal, E in FIG. 1 and A in FIG. 3. Sagane further discloses, "In FIGS. 3 and 1, like reference characters designate like or corresponding parts, and repetitive descriptions of the parts in FIG. 3 are omitted" (see, for

example, column 6, lines 4-6, emphasis added). That is to say, a plurality of comparators 8 is provided to address multiple bugs, and each comparator 8 outputs a coincidence signal.

Moreover, Hosotani expressly discloses a plurality of match circuits 9a-9c (see, for example, FIG. 2), each of which outputs a coincidence signal (see, for example, column 4, lines 38-43). Appellant does not dispute that the match circuits of Hosotani are analogous to the comparators of Sagane and that both are equated with the "coincidence detecting circuits" recited in claim 13.

Appellant further contends that "even if each of the pluralities of comparators 8 described at column 7, line 1 of Sagane would necessarily output a coincidence signal, the Office Action fails to clearly identify within the second embodiment of Sagane where and how the CPU 2 is to receive a plurality of coincidence signals, since signal A of comparator 8 found within figure 3 is applied to switch 23 and not to the CPU 2" (Brief, page 8, fifth paragraph).

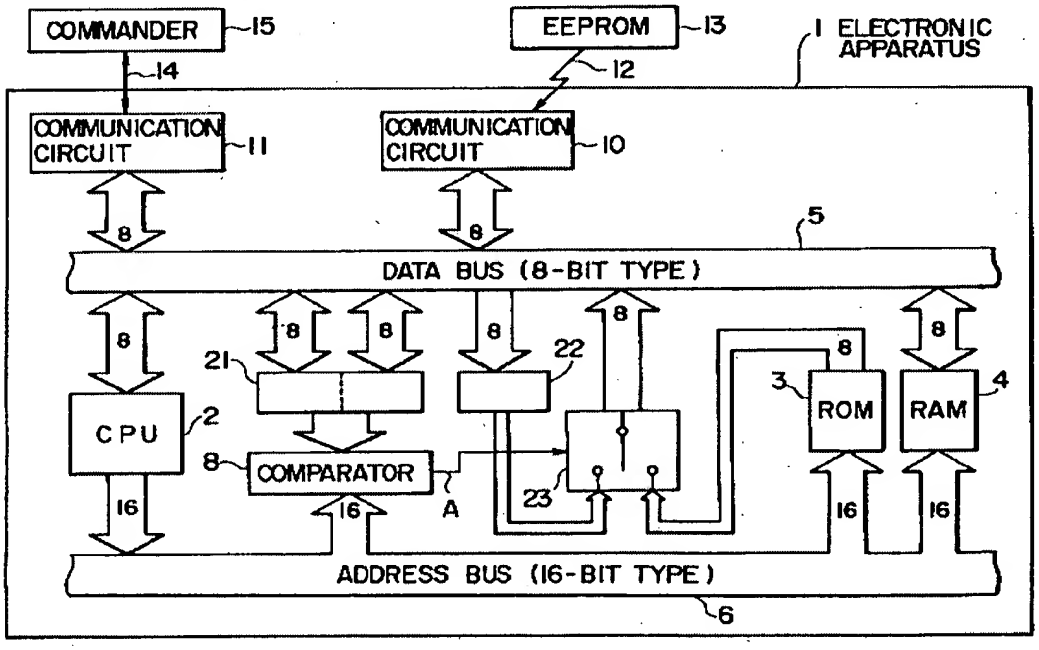
Here, Appellant appears to argue that such a "receiving" limitation should necessarily mean that the plurality of coincidence signals is directly connected or directly coupled to the CPU 2, as noted above.

However, the output of the comparator 8 determines which data the CPU 2 receives, as Sagane discloses (see, for example, column 6, lines 34-45, emphasis added):

> Next, the comparator 8 compares the execution address placed onto the address bus 6 with the correction address placed in the correction address register 21 (step S27). In case of a mismatch between the two addresses, the switch 23 is set to the ROM 3 position (step S34). As a result of access to the ROM 3 by the CPU 2, the data held in the ROM 3 are output therefrom onto the data bus 5 (step S35). If the execution address and the correction address coincide with each other, the switch 23 is set to the correction data register 22 position (step S28). This allows the correction data latched in the correction data register 22 to be output onto the data bus 5 (step S29).

Here, the switch 23 is the mechanism by which the CPU 2 "receives" the effect of the coincidence signal A from the comparator 8 (FIG. 3). Accordingly, Sagane indeed shows *where* and *how* the CPU 2 is to receive a plurality of coincidence signals: (1) from data held in the ROM 3 that is output onto the data bus 5 through the switch 23, or (2) from correction data latched in the correction data register 22 that is output onto the data bus 5 through the switch 23. Sagane's FIG. 3 is reproduced below.

FIG. 3

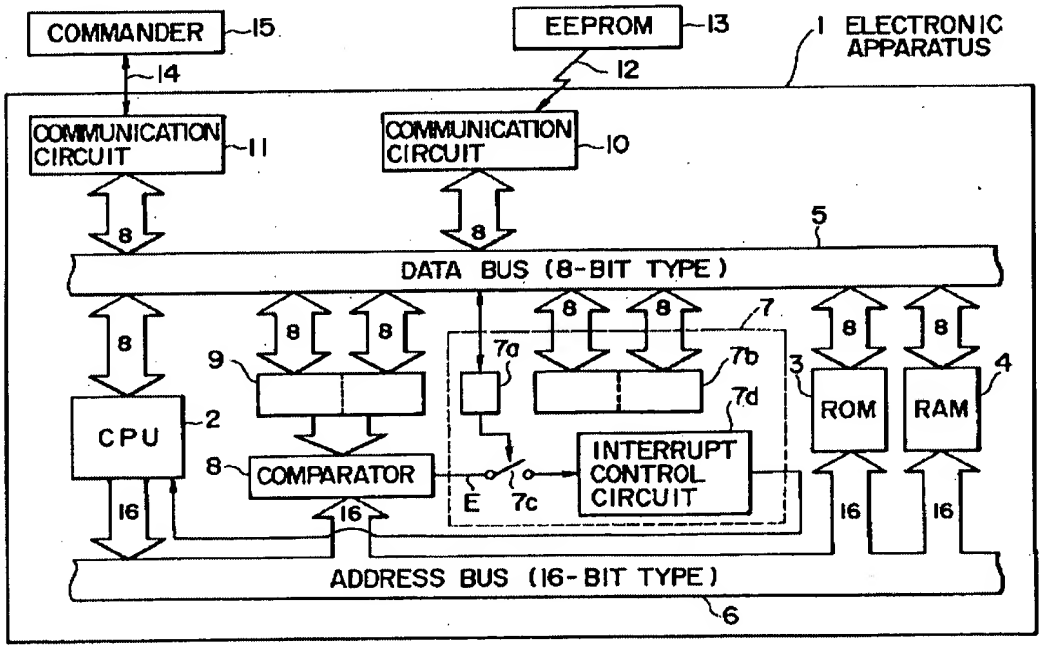


As noted above, claim 13 merely recites "a central processing unit receiving said plurality of coincidence signals" (emphasis added). The plain language of the claim does not include and/or exclude any such direct or indirect means for "receiving." Again, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Similarly, Appellant contends that the first embodiment of Sagane fails to show "where and how" the CPU 2 is to receive an interrupt (Brief, page 9, second paragraph), and specifically that "the first embodiment of Sagane fails to disclose, teach or suggest that an interrupt signal is provided from the interrupt control circuit 7d to the CPU 2" (Brief, page 10, first 4 lines).

However, Sagane expressly illustrates *where* and *how* the CPU 2 is to receive an interrupt (see, for example, FIG. 1). As illustrated, the CPU 2 receives the output of the interrupt control circuit 7d. Sagane expressly discloses that "the comparator 8 supplies the interrupt control circuit 7d with a coincidence signal E via the switch 7c, thereby generating an interrupt" (see, for example, column 5, lines 13-16, emphasis added). Sagane's FIG. 1 is reproduced below.

FIG. 1



Appellant further contends that "even if the first embodiment of Sagane teaches that an interrupt signal is provided from the interrupt control circuit 7d to the CPU 2, and even if the

first embodiment of Sagane suggests a plurality of coincidence signals E, the first embodiment of Sagane fails to disclose, teach or suggest the execution of a debugging program when one of the coincidence signals indicates a coincidence of the program address and the one of the plurality of bug addresses, along with the execution of another debugging program when another of the coincidence signals indicates a coincidence of the program address and the another of the plurality of bug addresses" (Brief, page 10, first paragraph).

However, Sagane discloses the execution of a correction program or "debugging program" when one of the coincidence signals indicates a coincidence of the execution address or "program address" and a correction address or "bug address" (see, for example, column 5, lines 8-21). In the case of a plurality of bugs, another correction program or "debugging program" is executed when the execution address or "program address" coincides with another correction address or "bug address" (see, for example, column 5, lines 49-54). Notwithstanding Appellant's allegation to the contrary (Brief, page 10, second paragraph), Sagane does teach a plurality of start addresses stored within the interrupt vector register 7b. Sagane expressly discloses "updating the interrupt generating address register 9 and the interrupt vector register 7b to reflect the next correction address and the start address of the next correction content, respectively" (see, for example, column 5, lines 51-54, emphasis added).

Appellant contends that the Office Action fails to provide some motivation as to why the skilled artisan would have substituted the switch 23 found within the second embodiment of Sagane with the access switching unit 7 found within the first embodiment of Sagane (Brief, pages 11, first 5 lines).

However, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

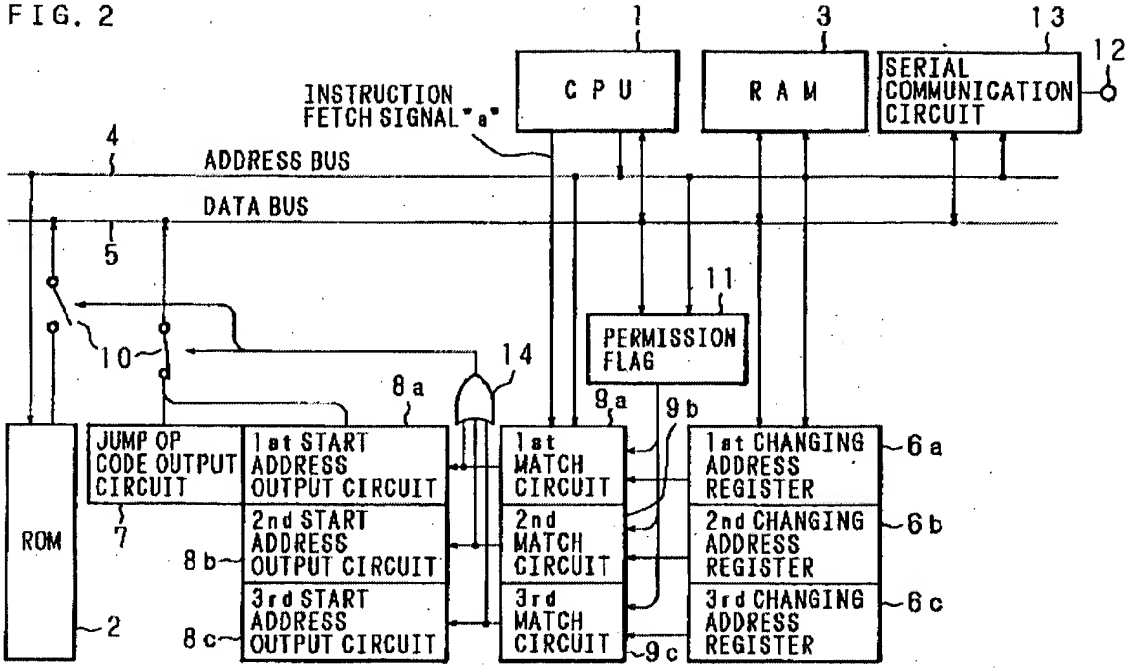
Here, Sagane teaches that the access switching unit 7 in FIG. 1 is a mechanism for switching access and execution from the ROM 3 (fixed storage means) to the RAM 4 (correction content storage means) (see, for example, column 5, lines 8-21). Likewise, Sagane teaches that the switch 23 in FIG. 3 is a mechanism for switching access and execution from the ROM 3 to the RAM 4 (see, for example, column 6, lines 37-52). Thus, the access switching unit 7 and the switch 23 are analogous mechanisms within the electronic apparatus 1 (see, for example, FIGS. 1 and 3). Indeed, Sagane expressly discloses that the electronic apparatus includes "access switching means for switching, when the comparing means outputs the coincidence signal, access by the processing means from the fixed storage means to the correction content storage means" (see, for example, column 2, lines 11-14). Again, it should be noted that in Sagane, the comparing means is the comparator 8, the processing means is the CPU 2, the fixed storage means is the ROM 3, and the correction content storage means is the RAM 4. And Sagane indeed suggests to the skilled artisan that the accessing switching means is implemented as the accessing switching unit 7 or equivalently as the switch 23. As stated at column 7, lines 3-6, "Another modification of the second embodiment is to interpose the control flag switch 7a and the switch 7c of FIG. 1 between the comparator 8 and the switch 23 in FIG. 3."

Furthermore, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Sagane expressly teaches both the access switching unit 7 and the switch 23.

Appellant contends that Hosotani fails to disclose, teach or suggest the output of OR circuit 14 being applied to CPU 1, and thus Hosotani fails to disclose, teach or suggest a central processing unit receiving a plurality of coincidence signals (Brief, page 12, first 5 lines).

However, Appellant acknowledges that "Hosotani arguably teaches that the output of OR circuit 14 is applied to switch 10 (Hosotani at figures 2, 6, 8, 10, 11)" (Brief, page 12, first 2 lines). Here, it should be noted that the output of the OR circuit 14, based on the output of the match circuits 9a-9c, determines which data the CPU 1 receives via the data bus 5 (see, for example, column 6, lines 34-39). The switch or connection control means 10 is the mechanism by which the CPU 1 "receives" the effect of the plurality of coincidence signals from the match circuits 9a-9c (see, for example, FIG. 2). Again, as noted above, claim 13 merely recites "a central processing unit receiving said plurality of coincidence signals" (emphasis added). The plain language of the claim does not include and/or exclude any such direct or indirect means for "receiving," and thus the argument is not persuasive. Hosotani's FIG. 2 is reproduced below.

FIG. 2



"Claim 19" (Brief, page 12).

In response to Appellant's argument, the rejections are based on the teachings of Sagane and Hosotani in combination, as noted above. Sagane also discloses that the CPU 2 "receives" a plurality of coincidence signals as separate interrupt requests (see, for example, column 5, lines 13-16 and 49-54), as set forth in the final Office Action (pages 13-14).

"Claim 20" (Brief, page 12).

In response to Appellant's argument, the rejections are based on the teachings of Sagane and Hosotani in combination, as noted above. Again, Hosotani discloses that the CPU 1 "receives" a plurality of coincidence signals as a single output from the OR circuit 14 (see, for example, column 4, line 60 to column 5, line 2), as set forth in the final Office Action (page 14).

The claim rejections set forth in the final Office Action mailed on November 19, 2004 are reproduced below for completeness:

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 13-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,454,100 to Sagane (art of record) in view of U.S. Pat. No. 5,701,506 to Hosotani (art of record).

With respect to claim 13 (previously presented), Sagane discloses a data processing apparatus performing predetermined data processing in accordance with instruction codes read from a program memory storing a program (see, for example, column 1, lines 9-14), the data processing apparatus comprising:

(a) a debugging circuit having a plurality of bug address setting registers and a plurality of coincidence detecting circuits (see, for example, column 6, line 67 to column 7, line 3, which shows a plurality of correction address registers, i.e. bug address setting registers, and a plurality of comparators, i.e. coincidence detecting circuits),

(i) one of said plurality of bug address setting registers holding one of a plurality of bug addresses that show the start of a buggy part of said program stored in said program memory (see, for example, column 6, lines 7-9, which shows a bug address setting register holding a correction address, and column 3, lines 32-34, which shows that such a correction address denotes the start of a buggy part of the program),

(ii) one of said plurality of coincidence detecting circuits comparing a program address for reading instruction codes from said program memory with said one of said plurality of bug addresses held in said one of said plurality of bug address setting registers, said one of said plurality of coincidence detecting circuits outputting one of a plurality of

coincidence signals when said program address and said one of said plurality of bug addresses coincide (see, for example, column 6, lines 34-37, which shows a coincidence detecting circuit comparing an execution address, i.e. a program address, with a bug address, and column 3, lines 48-52, which shows that such a coincidence detecting circuit outputs a coincidence signal when the addresses coincide),

(iii) another of said plurality of bug address setting registers holding another of said plurality of bug addresses that show the start of another buggy part of the program stored in the program memory (see, for example, column 6, lines 7-9, which shows a bug address setting register holding a correction address, i.e. another of the plurality of bug address setting registers holding another correction address, and column 3, lines 32-34, which shows that such a correction address denotes the start of a buggy part, i.e. another buggy part, of the program),

(iv) another of said plurality of coincidence detecting circuits comparing said program address for reading instruction codes from said program memory with said another of said plurality of bug addresses held in said another of said plurality of bug address setting registers, said another of said plurality of coincidence detecting circuits outputting another of said plurality of coincidence signals when said program address and said another of said plurality of bug addresses coincide (see, for example, column 6, lines 34-37, which shows a coincidence detecting circuit comparing an execution address with a bug address, i.e. another of the plurality of coincidence detecting circuits comparing a program address with a bug address, and column 3, lines 48-52, which shows that such a coincidence detecting circuit outputs a coincidence signal, i.e. another coincidence signal, when the addresses coincide); and

(b) a central processing unit (see, for example, CPU 2 in FIG. 3), wherein said central processing unit:

(i) executes one of a plurality of debugging programs stored within random access memory when said one of said plurality of coincidence signals indicates a coincidence of said program address and said one of said plurality of bug addresses (see, for example, column 6, lines 41-52, which shows executing a correction program stored within RAM, i.e. a debugging program, when the addresses coincide),

(ii) executes another of said plurality of debugging programs stored within said random access memory when said another of said plurality of coincidence signals indicates a coincidence of said program address and said another of said plurality of bug addresses (see, for example, column 6, lines 41-52, which shows executing a correction program stored within RAM, i.e. another debugging program, when the addresses coincide), and

(iii) executes said program stored within said program memory when said plurality of coincidence signals indicates a non-coincidence of

said program address and any of said plurality of bug addresses (see, for example, column 6, lines 37-40, which shows accessing ROM, i.e. executing the program stored within program memory, when there is no coincidence).

Although Sagane does not expressly disclose the limitation wherein the central processing unit receives a plurality of coincidence signals, the second embodiment of Sagane provides for a plurality of comparators or coincidence detecting circuits (see, for example, column 6, line 67 to column 7, line 3). Every such comparator disclosed by Sagane outputs a coincidence signal (see, for example, column 3, lines 48-52). It would have been apparent to one of ordinary skill in the art at the time the invention was made that the plurality of comparators would output a corresponding plurality of coincidence signals.

Furthermore, Hosotani discloses a plurality of changing address registers, i.e. bug address setting registers, and a plurality of match circuits, i.e. coincidence detecting circuits (see, for example, FIG. 2). Each match circuit outputs a signal representing the result of an address comparison, for the purpose of correcting a plurality of bugs in the program (see, for example, column 4, lines 30-59). Thus, Hosotani expressly discloses a plurality of coincidence signals. It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement Sagane with the features taught by Hosotani, for example to correct a plurality of bugs in ROM without incurring the expense of rebuilding the ROM (see, for example, Hosotani, column 1, lines 45-50).

In Hosotani, the plurality of coincidence signals is "applied" to CPU 1 of FIG. 2 in the sense that the coincidence signals apply the appropriate connections to the data bus of the CPU (see, for example, column 6, lines 34-39). Likewise, the CPU 1 of FIG. 2 "receives" the plurality of coincidence signals in the sense that the CPU receives data in accordance with those coincidence signals (see, for example, column 6, lines 1-19).

Moreover, Sagane further discloses that the coincidence signal may generate an interrupt to signal the CPU that the addresses coincide (see, for example, column 5, lines 13-16). In this case, the interrupt is the coincidence signal per se (see, for example, column 3, lines 59-61), and as illustrated in FIG. 1, the signal is clearly connected to CPU 2. The access switching unit 7 provides the interrupt for signaling coincidence (see, for example, column 3, lines 53-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second embodiment of Sagane such that access switching unit 7 of FIG. 1 substitutes for switch 23 of FIG. 3. The access switching unit 7 and the switch 23 are analogous means by which control is switched between the program in ROM and the correction program in RAM (see, for example, column 5, lines 8-21, and column 6, lines 41-52).

Therefore, Sagane discloses a plurality of coincidence detecting circuits, and suggests to one of ordinary skill in the art a corresponding plurality of coincidence signals. Sagane further discloses that the central processing unit may receive the coincidence signals as interrupts. Hosotani likewise discloses a

plurality of coincidence detecting circuits, and expressly discloses the plurality of coincidence signals. Hosotani further suggests that the coincidence signals are applied to the central processing unit, as presented above.

With respect to claim 14 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein an interrupt request for said central processing unit is generated when any of said plurality of coincidence signals indicates a coincidence of said program address and any of said plurality of bug addresses (see, for example, Sagane, column 5, lines 13-16, which shows generating an interrupt from the coincidence signal, i.e. any of the coincidence signals, when the corresponding addresses coincide).

Again, it would have been obvious to one of ordinary skill in the art to modify the second embodiment of Sagane such that access switching unit 7 of FIG. 1, which provides the interrupt for signaling coincidence (see, for example, column 3, lines 53-65), substitutes for switch 23 of FIG. 3. The access switching unit 7 and the switch 23 are analogous means by which control is switched between the program in ROM and the correction program in RAM (see, for example, column 5, lines 8-21, and column 6, lines 41-52).

With respect to claim 15 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein, when said one of said plurality of coincidence signals indicates said coincidence of said program address and said one of said plurality of bug addresses, said central processing unit:

(a) suspends execution of said program stored within said program memory after receiving said interrupt request (see, for example, Sagane, column 5, lines 11-20, which shows passing control to a correction program in RAM, i.e. suspending execution of the program in ROM, after receiving an interrupt request),

(b) processes an instruction stored within said random access memory at said one of said plurality of bug addresses to begin execution of said one of a plurality of debugging programs after suspending execution of said program (see, for example, Sagane, column 5, lines 17-21, which shows executing a correction program, i.e. a debugging program, at a correction address, i.e. a bug address, after suspending execution),

(c) suspends execution of said one of a plurality of debugging programs by processing an instruction residing within said one of a plurality of debugging programs that has a return address (see, for example, Sagane, column 5, lines 22-28, which shows returning to an address in ROM, i.e. suspending execution of a debugging program in RAM, by processing a jump instruction within the debugging program), and

(d) resumes execution of said program stored within said program memory by processing an instruction residing within said program memory at said return address (see, for example, Sagane, column 5, lines 25-31, which shows returning

control to the program in ROM, i.e. resuming execution of the program at the return address).

With respect to claim 16 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein, when said another of said plurality of coincidence signals indicates said coincidence of said program address and said another of said plurality of bug addresses, said central processing unit:

(a) suspends execution of said program stored within said program memory after receiving said interrupt request (see, for example, Sagane, column 5, lines 11-20, which shows passing control to a correction program in RAM, i.e. suspending execution of the program in ROM, after receiving an interrupt request),

(b) processes an instruction stored within said random access memory at said another of said plurality of bug addresses to begin execution of said another of a plurality of debugging programs after suspending execution of said program (see, for example, Sagane, column 5, lines 17-21, which shows executing a correction program at a correction address, i.e. another of the plurality of debugging programs at another of the plurality of bug addresses, after suspending execution),

(c) suspends execution of said another of a plurality of debugging programs by processing an instruction residing within said another of a plurality of debugging programs that has a return address (see, for example, Sagane, column 5, lines 22-28, which shows returning to an address in ROM, i.e. suspending execution of another of the plurality of debugging programs in RAM, by processing a jump instruction within the debugging program), and

(d) resumes execution of said program stored within said program memory by processing an instruction residing within said program memory at said return address (see, for example, Sagane, column 5, lines 25-31, which shows returning control to the program in ROM, i.e. resuming execution of the program at the return address).

With respect to claim 17 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said plurality of bug addresses is stored within said random access memory (see, for example, Sagane, column 5, lines 44-48, which shows that the correction address, i.e. the bug address, is stored in RAM, and lines 49-54, which shows that there is a plurality of such bug addresses).

With respect to claim 18 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said plurality of coincidence signals is a plurality of interrupt request signals (see, for example, Sagane, column 5, lines 13-16, which shows generating an interrupt request signal from

the coincidence signal, and lines 49-54, which shows that there is a plurality of such interrupt request signals).

Again, it would have been obvious to one of ordinary skill in the art to modify the second embodiment of Sagane such that access switching unit 7 of FIG. 1, which provides the interrupt for signaling coincidence (see, for example, column 3, lines 53-65), substitutes for switch 23 of FIG. 3. The access switching unit 7 and the switch 23 are analogous means by which control is switched between the program in ROM and the correction program in RAM (see, for example, column 5, lines 8-21, and column 6, lines 41-52).

With respect to claim 19 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said central processing unit receives said plurality of coincidence signals as separate interrupt requests (see, for example, Sagane, column 5, lines 13-16, which shows generating an interrupt request signal from the coincidence signal, and lines 49-54, which shows repeating the interrupt sequence separately for each bug, i.e. such that the CPU receives the plurality of coincidence signals as separate interrupt requests).

Again, it would have been obvious to one of ordinary skill in the art to modify the second embodiment of Sagane such that access switching unit 7 of FIG. 1, which provides the interrupt for signaling coincidence (see, for example, column 3, lines 53-65), substitutes for switch 23 of FIG. 3. The access switching unit 7 and the switch 23 are analogous means by which control is switched between the program in ROM and the correction program in RAM (see, for example, column 5, lines 8-21, and column 6, lines 41-52).

With respect to claim 20 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said central processing unit receives said plurality of coincidence signals as a single interrupt request (see, for example, Sagane, column 5, lines 13-16, which shows generating an interrupt request signal from the coincidence signal, and lines 49-54, which shows that there is a plurality of such interrupt request signals; further see, for example, Hosotani, column 4, line 60 to column 5, line 2, which shows that the plurality of coincidence signals becomes a single output signal).

Again, it would have been obvious to one of ordinary skill in the art to modify the second embodiment of Sagane such that access switching unit 7 of FIG. 1, which provides the interrupt for signaling coincidence (see, for example, column 3, lines 53-65), substitutes for switch 23 of FIG. 3. The access switching unit 7 and the switch 23 are analogous means by which control is switched between the program in ROM and the correction program in RAM (see, for example, column 5, lines 8-21, and column 6, lines 41-52).

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement Sagane with the features taught by Hosotani, for example to correct a plurality of bugs in ROM without incurring

the expense of rebuilding the ROM (see, for example, Hosotani, column 1, lines 45-50).

With respect to claim 21 (previously presented), although Sagane in view of Hosotani discloses the limitation wherein said plurality of coincidence signals are input to said central processing unit as an interrupt request signal (see, for example, Sagane, column 5, lines 13-16, which shows generating an interrupt request signal from the coincidence signal, and lines 49-54, which shows that there is a plurality of such interrupt request signals), Sagane in view of Hosotani does not expressly disclose the limitation wherein said plurality of coincidence signals are logically AND'ed together.

However, Hosotani discloses that the coincidence signals are logically OR'ed together, and that the resulting output is at a "1" level when any one of the address comparisons is a match and at a "0" level when all of the comparisons are mismatches (see, for example, column 4, line 60 to column 5, line 2). In other words, Hosotani defines the coincidence detection circuitry as active high. When the signals are instead defined as active low, the same result is achieved by substituting the OR gate with an AND gate, as is well known in the art. The resulting output from the AND gate, in this case, would then be at a "0" level when any one of the address comparisons is a match and at a "1" level when all of the comparisons are mismatches.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the logical OR operation disclosed by Hosotani with a logical AND operation when the coincidence detection circuitry is defined as active low, rather than active high as taught by Hosotani, to achieve an equivalent result.

With respect to claim 22 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said plurality of debugging programs are input during initialization into said random access memory from a source external to said data processing apparatus (see, for example, Sagane, column 3, lines 32-46, which shows inputting the correction content, i.e. the plurality of debugging programs, into RAM from an external EEPROM during initialization).

With respect to claim 23 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said random access memory stores a plurality of interrupt vectors of start addresses, said start addresses identifying memory areas within said random access memory that contain said plurality of debugging programs (see, for example, Sagane, column 5, lines 44-48, which shows that the start address is stored in RAM, and lines 49-54, which shows that there is a plurality of such start addresses that are interrupt vectors corresponding to the locations of a plurality of debugging programs in RAM).

With respect to claim 24 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said central processing unit suspends an instruction being executed and reads an instruction code from a program address designated by a predetermined address table when said central processing unit executes any of said plurality of debugging programs stored within random access memory (see, for example, Sagane, column 6, lines 41-52, which shows reading instruction data from an address referenced by a predetermined address table and executing a correction program stored within RAM, i.e. any of the plurality of debugging programs).

With respect to claim 25 (previously presented), Sagane in view of Hosotani further discloses the limitation wherein said program memory is read only memory (see, for example, Sagane, column 1, lines 9-14, which shows that the program is stored in ROM).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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